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**On pipelining dynamic instruction scheduling logic - all 9 versions »**

J Stark, MD Brown, YN Patt - Proceedings of the 33rd annual ACM/IEEE international ..., 2000 - portal.acm.org

... chain ADD  $\neq$  LOAD  $\neq$  OR using 2-cycle pipelined **scheduling** logic ... The ADD **instruction** wakes up in cycle 1 and is ... 1-cycle latency, so the LOAD's **DELAY** field is ...

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**Global instruction scheduling for superscalar machines**

D Bernstein, M Rodeh - Proceedings of the ACM SIGPLAN 1991 conference on ..., 1991 - portal.acm.org

... is no problem to activate the **instruction scheduling** after the register allocation is completed. 2 3 More precisely, usually the three cycle **delay** between a ...

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**Efficient instruction scheduling for a pipelined architecture - all 8 versions »**

PB Gibbons, SS Muchnick - Proceedings of the 1986 SIGPLAN symposium on Compiler ..., 1986 - portal.acm.org

... We implemented the **instruction scheduler** described above in C, adding to it a branch **scheduler** and a ... The branch **scheduler** attempts to fill **delay** slots fol ...

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**Speculation techniques for improving load related instruction scheduling - all 16 versions »**

A Yoaz, M Erez, R Ronen, S Jourdan - ACM SIGARCH Computer Architecture News, 1999 - portal.acm.org

... Load **instruction** latencies, on the other hand, vary ... to a lower hierarchy results in a longer **delay**. ... and reduces the efficiency of **scheduling** load dependent ...

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**[book] Integrating register allocation and instruction scheduling for RISCs**

DG Bradlee, SJ Eggers, RR Henry - 1991 - ACM Press New York, NY, USA

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**Select-Free Instruction Scheduling Logic - all 18 versions »**

M Brown, J Stark, Y Patt - Proceedings of the 34th Annual International Symposium on ..., 2001 - doi.ieeecomputersociety.org

... The need to prioritize all ready **instructions** adds to the **delay** in the **scheduling** loop; by removing the priori- tization and performing selection in a ...

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**IMPACT: an architectural framework for multiple-instruction-issue processors - all 7 versions »**

PP Chang, SA Mahlke, WY Chen, NJ Warter, WH Wen- ... - ACM SIGARCH Computer Architecture News, 1991 - portal.acm.org

... par- allelism. In processors with hardware support for dynamic code **scheduling**, the scope of **instruction scheduling** is lim- ited ...

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**Cyclone: a broadcast-free dynamic instruction scheduler with selective replay - all 12 versions »**

D Ernst, A Hamel, T Austin - Computer Architecture, 2003. Proceedings. 30th Annual ..., 2003 -  
ieeexplore.ieee.org

... with each store set identifier the **delay** until the ... When **scheduling** stores, the latency  
of a store operation ... a store value to a load **instruction**, typically the ...

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### Dynamic instruction scheduling and the Astronautics ZS-1 - all 7 versions »

JE Smith - Computer, 1989 - ieeexplore.ieee.org

... and hardware can be kept simple by doing as much as possible in software." A corollary  
naturally fol- lows, stating that **instruction scheduling** should be ...

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### Conflict modelling and instruction scheduling in code generation for in-house DSP cores - all 13 versions »

AH Timmer, MTJ Strik, JL van Meerbergen, JAG Jess - Proceedings of the 32nd ACM/IEEE conference  
on Design ..., 1995 - portal.acm.org

... The examples range from a simple **delay** line to a portable audio application (which  
is a real life industry example). The **instruction-set scheduler** based on ...

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